

## CLAIMS

1           1.     A high-speed digital transmitter capable of sending side channel data, the  
2 transmitter comprising:  
3                 a channel zero encoder having first and second inputs and an output, the first  
4                     input receiving channel zero primary data, the second input receiving a  
5                     channel zero DE<sub>out</sub> signal, and the output producing channel zero encoded  
6                     data, the channel zero encoder operative to produce channel zero encoded  
7                     data based at least in part on the channel zero primary data and the channel  
8                     zero DE<sub>out</sub> signal;  
9                 a channel one multiplexer having at least first and second data inputs, at least one  
10                    control input, and at least one output, the channel one multiplexer  
11                    operative to multiplex channel one primary data and channel one side  
12                    channel data, the first data input receiving channel one primary data, the  
13                    second data input receiving channel one side channel data, the control  
14                    input receiving a DEI signal, and the output providing a multiplexed signal  
15                    including channel one side channel data and channel one primary data;  
16                 channel one DE<sub>out</sub> control logic having a first input and an output, the channel one  
17                    DE<sub>out</sub> control logic operative to produce a channel one DE<sub>out</sub> signal for  
18                    facilitating the transfer of channel one side channel data, the first input  
19                    receiving a DEI signal, and the output producing a channel one DE<sub>out</sub>  
20                    signal; and  
21                 a channel one encoder having first and second inputs and an output, the first input  
22                    receiving the output of the channel one multiplexer, the second input

23 receiving the output of the channel one DE<sub>out</sub> control logic, the output  
24 producing channel one encoded data, the channel one encoder operative to  
25 produce channel one encoded data based at least in part on the first and  
26 second inputs.

1 2. The transmitter of claim 1, wherein the channel zero DE<sub>out</sub> signal is the DEI  
2 signal.

1 3. The transmitter of claim 1, wherein the channel zero encoder has third and fourth  
2 inputs for receiving Hsync and Vsync signals.

3 4. The transmitter of claim 1, wherein the transmitter further comprises:  
4 a channel two multiplexer having at least first and second data inputs, a control  
5 input, and an output, the channel two multiplexer operative to multiplex  
6 channel two primary data and channel two side channel data, the first data  
7 input receiving channel two primary data, the second data input receiving  
8 channel two side channel data, the control input receiving a DEI signal,  
9 and the output providing channel two side channel data or channel two  
10 primary data depending on the value of the DEI signal;  
11 channel two DE<sub>out</sub> control logic having an input and an output, the channel two  
12 DE<sub>out</sub> control logic operative to produce a channel two DE<sub>out</sub> signal for  
13 facilitating the transfer of channel two side channel data, the first input  
receiving a DEI signal, and the output producing a channel two DE<sub>out</sub>  
signal; and

14 a channel two encoder having first and second inputs and an output, the first input  
15 receiving the output of the channel two multiplexer, the second input  
16 receiving the output of the channel two DE<sub>out</sub> control logic, the output  
17 producing channel two encoded data, the channel two encoder operative to  
18 produce channel two encoded data based at least in part on the first and  
19 second inputs.

1 5. The transmitter of claim 1, wherein the transmitter further comprises:

2 a channel one FIFO having an input for receiving channel one side channel data  
3 and an output coupled to the second data input of the channel one  
4 multiplexer, the output providing channel one side channel data to the  
5 channel one multiplexer.

6 6. The transmitter of claim 1, wherein the channel one encoder has third and forth  
7 inputs, the third input receiving a first control signal and the fourth input receiving a second  
8 control signal, and

9 wherein the channel one DE<sub>out</sub> control logic has second and third inputs, the second input  
10 receiving the first control signal, and the third input receiving the second control signal.

1 7. The transmitter of claim 6, wherein the channel one DE<sub>out</sub> control logic  
2 comprises:

3 a first control signal transition indication logic having an input and an output, the  
4 input adapted to receive the first control signal, the output providing a de-  
5 asserted signal as a result of a transition in the first control signal;

6 a second control signal transition indication logic having an input and an output,  
7 the input adapted to receive the second control signal, the output providing  
8 a de-asserted signal as a result of a transition in the second control signal;  
9 DE<sub>out</sub> inter-channel synchronization compliance logic having an input and an  
10 output, the input adapted to receive the DEI signal, the output providing a  
11 de-asserted period of a preselected length and at a preselected location  
12 relative to a de-asserted period in the DEI signal; and  
13 An AND gate having first, second and third inputs and an output, the first input  
14 being coupled to the output of the first control signal transition indication  
15 logic, the second input being coupled to the output of the second control  
16 signal transition indication logic, the third input being coupled to the  
17 output of the DE<sub>out</sub> inter-channel synchronization compliance logic, the  
18 output providing a digital visual interface compliant DE<sub>out</sub> signal.

19  
20  
21 8. The transmitter of claim 7, wherein the first control signal transition indication  
22 logic comprises

23 a first delay element having an input and an output, the input adapted to receive  
24 the first control signal, the output producing a first delayed control signal;  
25 a first logic gate having first and second inputs and an output, the first logic gate  
26 providing a de-asserted signal as a result of a transition of the first control  
27 signal, the first input coupled to the output of the first delay element, the  
28 second input adapted to receive the first control signal; and

29 wherein the second control signal transition indication logic comprises

10 a second delay element having an input and an output, the input adapted to  
11 receive the second control signal, the output producing a second delayed  
12 control signal;  
13 a second logic gate having first and second inputs and an output, the second logic  
14 gate providing a de-asserted signal as a result of a transition of the second  
15 control signal, the first input coupled to the output of the second delay  
16 element, the second input adapted to receive the second control signal.

1 9. The transmitter of claim 7, wherein the channel one DEout control logic further  
2 comprises:  
3 phase-tracking compliance logic having an input and an output, the input adapted  
4 to receive the DEI signal, the output providing a de-asserted signal as a  
5 result of a transition in the DEI signal.

6 10. The transmitter of claim 9, wherein the phase tracking compliance logic  
7 comprises:  
8 a delay element having an input and an output, the input adapted to receive the  
9 DEI signal, the output producing a delayed DEI signal;  
10 an inverter having an input and an output, the input adapted to receive the DEI  
signal, and the output producing an inverted DEI signal; and  
a NAND gate having first and second inputs and an output, the first input coupled  
to the output of the delay element, the second input coupled to the output  
of the inverter, the output producing a low period as a result of a transition  
from high to low in the DEI signal.

1           11.    A high-speed digital receiver capable of receiving side channel data, the receiver  
2 comprising:  
3           a channel zero decoder having a first input and first and second outputs, the first  
4                 input receiving channel zero encoded data, the first output producing a  
5                 channel zero decoded data signal, the second output producing a channel  
6                 zero DE<sub>out</sub> signal, the channel zero decoder operative to produce channel  
7                 zero decoded data and a channel zero DE<sub>out</sub> signal from the channel zero  
8                 encoded data;  
9           a channel one decoder having at least an input and first and second outputs, the  
10                 first input receiving channel one encoded data, the first output producing  
11                 channel one decoded data, the second output producing a channel one  
12                 DE<sub>out</sub> signal, the channel one decoder operative to produce channel one  
13                 decoded data and a channel one DE<sub>out</sub> signal from the channel one  
14                 encoded data;  
15           DEI signal and FIFO control signal recovery logic having first and second inputs  
16                 and first and second outputs, the first input receiving the channel zero  
17                 DE<sub>out</sub> signal, the second input receiving the channel one DE<sub>out</sub> signal, the  
18                 DEI signal and FIFO control signal recovery logic operative to derive a  
19                 DEI signal, the first output producing a DEI signal, the second output  
20                 producing a first FIFO control signal; and  
21           a channel one de-multiplexer having a data input, a control input, and first and  
22                 second outputs, the channel one de-multiplexer operative to separate  
23                 channel one decoded data into channel one primary data and channel one

24 side channel data, the data input receiving channel one decoded data from  
25 the channel one decoder, the control input receiving the DEI signal from  
26 the DEI signal and FIFO control signal recovery logic, the first output  
27 producing channel one side channel data, and the second output producing  
28 channel one primary data.

1 12. The receiver of claim 11, wherein the receiver further comprises:  
2 a channel two decoder having at least one input and at least first and second  
3 outputs, the first input receiving channel two encoded data, the first output  
4 producing channel two decoded data, the second output producing a  
5 channel two DE<sub>out</sub> signal, the channel two decoder operative to produce  
6 channel two decoded data and a channel two DE<sub>out</sub> signal from the channel  
7 two encoded data;  
8 a channel two de-multiplexer having a data input, a control input, and first and  
9 second outputs, the channel two de-multiplexer operative to separate  
10 channel two decoded data into channel two primary data and channel two  
11 side channel data, the data input receiving channel two decoded data from  
12 the channel two decoder, the control input receiving the DEI signal from  
13 the DEI signal and FIFO control signal recovery logic, the first output  
14 producing channel two side channel data, and the second output producing  
15 channel two primary data.

1 13. The receiver of claim 12, wherein the DEI signal and FIFO control signal recovery  
2 logic comprises:

3 a first AND gate having first second and third inputs and an output, the first input  
4 adapted to receive the channel zero DE<sub>out</sub> signal from the channel zero  
5 decoder, the second input adapted to receive the channel one DE<sub>out</sub> signal  
6 from the channel one decoder, the third input adapted to receive the  
7 channel two DE<sub>out</sub> signal from the channel two decoder, the output  
8 providing the DEI signal;  
9 an inverter having an input and an output, the input coupled to the output of the  
10 first AND gate to receive the DEI signal, the output providing an inverted  
11 DEI signal;  
12 a second AND gate having first and second inputs and an output, the first input  
13 coupled to the output of the inverter to receive the inverted DEI signal, the  
14 second input adapted to receive the channel one DE<sub>out</sub> signal from the  
15 channel one decoder, the output providing a channel one FIFO control  
16 signal; and  
17 a third AND gate having first and second inputs and an output, the first input  
18 coupled to the output of the inverter to receive the inverted DEI signal, the  
19 second input adapted to receive the channel two DE<sub>out</sub> signal from the  
20 channel two decoder, the output providing a channel two FIFO control  
21 signal.

1 14. The receiver of claim 13, wherein the receiver further comprises:

2 a channel one FIFO having a data input, a control input and an output, the data  
3 input coupled to the first output of the channel one de-multiplexer, the  
4 control input adapted to receive the channel one FIFO control signal from



5 the second AND gate, and the output providing channel one side channel  
6 data; and  
7 a channel two FIFO having a data input, a control input and an output, the data  
8 input coupled to the first output of the channel two de-multiplexer, the  
9 control input adapted to receive the channel two FIFO control signal from  
10 the third AND gate, and the output providing channel two side channel  
11 data.

- 1 15. A method for sending side channel data, the method comprising:  
2 encoding channel zero primary data for transmission using a channel zero encoder  
3 having first and second inputs and one output, the first input receiving  
4 channel zero primary data, the second input receiving a channel zero  $DE_{out}$   
5 signal, and the output producing channel zero encoded data, the channel  
6 zero encoder operative to produce channel zero encoded data based at  
7 least in part on the channel zero primary data and the channel zero  $DE_{out}$   
8 signal;  
9 multiplexing channel one primary data and channel one side channel data using a  
10 channel one multiplexer having first and second data inputs, a control  
11 input, and an output, the first data input receiving channel one primary  
12 data, the second data input receiving channel one side channel data, the  
13 control input receiving a DEI signal, and the output providing channel one  
14 side channel data or channel one primary data depending on the value of  
15 the DEI signal;

16 producing a channel one DE<sub>out</sub> signal for facilitating the transfer of channel one  
17 side channel data using channel one DE<sub>out</sub> control logic having an input  
18 and an output, the first input receiving a DEI signal, and the output  
19 producing a channel one DE<sub>out</sub> signal; and  
20 encoding channel one data for transmission using a channel one encoder having  
21 first and second inputs and an output, the first input receiving the output of  
22 the channel one multiplexer, the second input receiving the output of the  
23 channel one DE<sub>out</sub> control logic, the output producing channel one  
24 encoded data based at least in part on the two inputs.

- 1 16. A method for receiving side channel data, the method comprising:  
2 receiving channel zero encoded data and channel one encoded data;  
3 decoding channel zero encoded data using a channel zero decoder having a first  
4 input and first and second outputs, the first input receiving channel zero  
5 encoded data, the first output producing a channel zero decoded data  
6 signal, the second output producing a channel zero DE<sub>out</sub> signal;  
7 decoding channel one encoded data using a channel one decoder having at least  
8 an input and first and second outputs, the first input receiving channel one  
9 encoded data, the first output producing channel one decoded data, the  
10 second output producing a channel one DE<sub>out</sub> signal;  
11 deriving a DEI signal using DEI signal and FIFO control signal recovery logic  
12 having first and second inputs and first and second outputs, the first input  
13 receiving the channel zero DE<sub>out</sub> signal, the second input receiving the

channel one DE<sub>out</sub> signal, the first output producing a DEI signal, the  
second output producing a first FIFO control signal; and  
separating channel one decoded data from channel one side channel data using a  
channel one de-multiplexer having a data input, a control input, and first  
and second outputs, the data input receiving channel one decoded data  
from the channel one decoder, the control input receiving the DEI signal  
from the DEI signal and FIFO control signal recovery logic, the first  
output producing channel one side channel data, and the second output  
producing channel one primary data.

17. A high speed digital transmission system capable of sending side channel, the  
system comprising:

a transmitter having first and second outputs,  
a receiver having first and second inputs,  
channel zero connecting the first output of the transmitter to the first input of the  
receiver, and  
channel one connecting the second output of the transmitter to the second input of  
the receiver;

wherein the transmitter comprises:

a channel zero encoder having first and second inputs and an output, the  
first input receiving channel zero primary data, the second input  
receiving a channel zero DE<sub>out</sub> signal, and the output producing  
channel zero encoded data, the channel zero encoder operative to

14 produce channel zero encoded data based at least in part on the  
15 channel zero primary data and the channel zero DE<sub>out</sub> signal;  
16 a channel one multiplexer having first and second data inputs, a control  
17 input, and an output, the channel one multiplexer operative to  
18 multiplex channel one primary data and channel one side channel  
19 data, the first data input receiving channel one primary data, the  
20 second data input receiving channel one side channel data, the  
21 control input receiving a DEI signal, and the output providing  
22 channel one side channel data or channel one primary data  
23 depending on the value of the DEI signal;  
24 channel one DE<sub>out</sub> control logic having an input and an output, the channel  
25 one DE<sub>out</sub> control logic operative to produce a channel one DE<sub>out</sub>  
26 signal for facilitating the transfer of channel one side channel data,  
27 the first input receiving a DEI signal, and the output producing a  
28 channel one DE<sub>out</sub> signal; and  
29 a channel one encoder having two inputs and one output, the first input  
30 receiving the output of the channel one multiplexer, the second  
31 input receiving the output of the channel one DE<sub>out</sub> control logic,  
32 the output producing channel one encoded data the channel one  
33 encoder operative to produce channel one encoded data based at  
34 least in part on the two inputs; and  
35 wherein the receiver comprises:

36 a channel zero decoder having an input and first and second outputs, the  
37 first input receiving channel zero encoded data, the first output  
38 producing a channel zero decoded data signal, the second output  
39 producing a channel zero DE<sub>out</sub> signal, the channel zero decoder  
40 operative to produce channel zero decoded data and a channel zero  
41 DE<sub>out</sub> signal from the channel zero encoded data;  
42 a channel one decoder having at least one input and at least first and  
43 second outputs, the first input receiving channel one encoded data,  
44 the first output producing channel one decoded data, the second  
45 output producing a channel one DE<sub>out</sub> signal, the channel one  
46 decoder operative to produce channel one decoded data and a  
47 channel one DE<sub>out</sub> signal from the channel one encoded data;  
48 DEI signal and FIFO control signal recovery logic having first and second  
49 inputs and first and second outputs, the first input receiving the  
50 channel zero DE<sub>out</sub> signal, the second input receiving the channel  
51 one DE<sub>out</sub> signal, the DEI signal and FIFO control signal recovery  
52 logic operative to derive a DEI signal, the first output producing a  
53 DEI signal, the second output producing a first FIFO control  
54 signal; and  
55 a channel one de-multiplexer having a data input, a control input, and first  
56 and second outputs, the channel one de-multiplexer operative to  
57 separate channel one decoded data into channel one primary data  
58 and channel one side channel data, the data input receiving channel

one decoded data from the channel one decoder, the control input receiving the DEI signal from the DEI signal and FIFO control signal recovery logic, the first output producing channel one side channel data, and the second output producing channel one primary data.

18. A high-speed digital transmitter capable of sending side channel data, the transmitter comprising:

channel zero encoder means for producing channel zero encoded data, said

channel zero encoder means having first and second inputs and an output, the first input receiving channel zero primary data, the second input receiving a channel zero  $DE_{out}$  signal, and the output producing channel zero encoded data based at least in part on the channel zero primary data and the channel zero  $DE_{out}$  signal;

channel one multiplexing means for multiplexing channel one primary data and

channel one side channel data, said channel one multiplexing means having first and second data inputs, a control input, and an output, the first data input receiving channel one primary data, the second data input receiving channel one side channel data, the control input receiving a DEI signal, and the output providing channel one side channel data or channel one primary data depending on the value of the DEI signal;

channel one  $DE_{out}$  control logic means for producing a channel one  $DE_{out}$  signal

for facilitating the transfer of channel one side channel data, said channel one  $DE_{out}$  control logic means having an input and an output, the first

19 input receiving a DEI signal, and the output producing a channel one DE<sub>out</sub>  
20 signal; and  
21 channel one encoding means for producing channel one encoded data, said  
22 channel one encoding means having first and second inputs and an output,  
23 the first input receiving the output of the channel one multiplexer, the  
24 second input receiving the output of the channel one DE<sub>out</sub> control logic,  
25 the output producing channel one encoded data based at least in part on  
26 the two inputs.

1 19. The transmitter of claim 18, wherein the channel zero encoder means has third  
2 and fourth inputs for receiving Hsync and Vsync signals.  
3  
4 20. The transmitter of claim 18, wherein the transmitter further comprises:  
5 a channel one FIFO having an input for receiving channel one side channel data  
6 and an output coupled to the second data input of the channel one  
7 multiplexing means, the output providing channel one side channel data to  
8 the multiplexing means.

1 21. A high-speed digital receiver capable of receiving side channel data, the receiver  
2 comprising:  
3 channel zero decoder means for producing channel zero decoded data and a  
4 channel zero DE<sub>out</sub> signal, said channel zero decoder means having an  
5 input and first and second outputs, the first input receiving channel zero  
6 encoded data, the first output producing a channel zero decoded data  
7 signal, the second output producing a channel zero DE<sub>out</sub> signal;

8 channel one decoder means for producing channel one decoded data and a  
9 channel one DE<sub>out</sub> signal, said channel one decoder means having at least  
10 one input and at least first and second outputs, the first input receiving  
11 channel one encoded data, the first output producing channel one decoded  
12 data, the second output producing a channel one DE<sub>out</sub> signal;  
13 DEI signal and FIFO control signal recovery logic means for deriving a DEI  
14 signal, said DEI signal and FIFO control signal recovery logic means  
15 having first and second inputs and first and second outputs, the first input  
16 receiving the channel zero DE<sub>out</sub> signal, the second input receiving the  
17 channel one DE<sub>out</sub> signal, the first output producing a DEI signal, the  
18 second output producing a first FIFO control signal; and  
19 de-multiplexing means for separating a data signal into channel one primary data  
20 and channel one side channel data, said de-multiplexing means having a  
21 data input, a control input, and first and second outputs, the data input  
22 receiving channel one decoded data from the channel one decoder, the  
23 control input receiving the DEI signal from the DEI signal and FIFO  
24 control signal recovery logic, the first output producing channel one side  
25 channel data, and the second output producing channel one primary data.

1 22. A method for sending side channel data over a communication link having  
2 a transmitter, a receiver, and at least a channel zero and a channel one connecting the transmitter  
3 and the receiver, the method comprising:



4 encoding channel zero primary data, and DEI data as in-band and out-of-band  
5 characters for transmission on channel zero;  
6 deriving a channel one DEout signal using channel one DE<sub>out</sub> control logic having  
7 an input and an output, the first input receiving a DEI signal, and the  
8 output producing a channel one DE<sub>out</sub> signal for facilitating the transfer of  
9 channel one side channel data;  
10 encoding channel one primary data, channel one side channel data, and DE<sub>out</sub>  
11 signal data for transmission on channel one, the encoding performed using  
12 in-band and out-of-band characters.

23. The method of claim 22, wherein the method further comprises:  
selecting which channel will carry a substantially unaltered DE signal based on a  
characterization of the channels.
24. The method of claim 22, wherein the method further comprises:  
communicating the capabilities of a receiver to a transmitter through a handshake  
procedure.
25. The method of claim 22, wherein deriving a channel one DEout signal comprises:  
adjusting the length of a data inactive period within the channel one DEout signal  
based on a characterization of the channel.
26. A high-speed digital transmitter capable of sending side channel data, the  
transmitter comprising:

3 a channel zero encoder having first , second, third, and fourth inputs and an  
4 output, the first input receiving channel zero primary data, the second  
5 input receiving a DEI signal, the third input receiving an Hsync signal, the  
6 fourth input receiving a Vsync signal, and the output producing channel  
7 zero encoded data, the channel zero encoder operative to produce channel  
8 zero encoded data based at least in part on the channel zero primary data,  
9 the DEI signal, the Hsync signal, and the Vsync signal;  
10 a channel one FIFO having an input for receiving channel one side channel data  
11 and an output for providing channel one side channel data;  
12 a channel one multiplexer having at least first and second data inputs, at least one  
13 control input, and at least one output, the channel one multiplexer  
14 operative to multiplex channel one primary data and channel one side  
15 channel data, the first data input receiving channel one primary data, the  
16 second data input coupled to the output of the channel one FIFO for  
17 receiving channel one side channel data, the control input receiving a DEI  
18 signal, and the output providing a multiplexed signal including channel  
19 one side channel data and channel one primary data;  
20 channel one DE<sub>out</sub> control logic having a first input and an output, the channel one  
21 DE<sub>out</sub> control logic operative to produce a channel one DE<sub>out</sub> signal for  
22 facilitating the transfer of channel one side channel data, the first input  
23 receiving a DEI signal, and the output producing a channel one DE<sub>out</sub>  
24 signal; and

25 a channel one encoder having first and second inputs and an output, the first input  
26 receiving the output of the channel one multiplexer, the second input  
27 receiving the output of the channel one DE<sub>out</sub> control logic, the output  
28 producing channel one encoded data, the channel one encoder operative to  
29 produce channel one encoded data based at least in part on the first and  
30 second inputs.

1 27. A high-speed digital receiver capable of receiving side channel data, the receiver  
2 comprising:

3 a channel zero decoder having a first input and first and second outputs, the first  
4 input receiving channel zero encoded data, the first output producing a  
5 channel zero decoded data signal, the second output producing a channel  
6 zero DE<sub>out</sub> signal, the channel zero decoder operative to produce channel  
7 zero decoded data and a channel zero DE<sub>out</sub> signal from the channel zero  
8 encoded data;

9 a channel one decoder having at least an input and first and second outputs, the  
10 first input receiving channel one encoded data, the first output producing  
11 channel one decoded data, the second output producing a channel one  
12 DE<sub>out</sub> signal, the channel one decoder operative to produce channel one  
13 decoded data and a channel one DE<sub>out</sub> signal from the channel one  
14 encoded data;

15 DEI signal and FIFO control signal recovery logic having first and second inputs  
16 and first and second outputs, the first input receiving the channel zero  
17 DE<sub>out</sub> signal, the second input receiving the channel one DE<sub>out</sub> signal, the

DEI signal and FIFO control signal recovery logic operative to derive a DEI signal, the first output producing a DEI signal, the second output producing a first FIFO control signal; wherein the DEI signal and FIFO control signal recovery logic comprises:

a first AND gate having first second and third inputs and an output, the first input adapted to receive the channel zero  $DE_{out}$  signal from the channel zero decoder, the second input adapted to receive the channel one  $DE_{out}$  signal from the channel one decoder, the third input adapted to receive the channel two  $DE_{out}$  signal from the channel two decoder, the output providing the DEI signal;

an inverter having an input and an output, the input coupled to the output of the first AND gate to receive the DEI signal, the output providing an inverted DEI signal;

a second AND gate having first and second inputs and an output, the first input coupled to the output of the inverter to receive the inverted DEI signal, the second input adapted to receive the channel one  $DE_{out}$  signal from the channel one decoder, the output providing a channel one FIFO control signal; and

a third AND gate having first and second inputs and an output, the first input coupled to the output of the inverter to receive the inverted DEI signal, the second input adapted to receive the channel two  $DE_{out}$  signal from the channel two decoder, the output providing a channel two FIFO control signal, and

41 a channel one de-multiplexer having a data input, a control input, and first  
42 and second outputs, the channel one de-multiplexer operative to  
43 separate channel one decoded data into channel one primary data  
44 and channel one side channel data, the data input receiving channel  
45 one decoded data from the channel one decoder, the control input  
46 receiving the DEI signal from the DEI signal and FIFO control  
47 signal recovery logic, the first output producing channel one side  
48 channel data, and the second output producing channel one  
49 primary data.